CE-ATA Technical Errata

Errata ID	**Protocol 001**
Affected Spec Ver.	**Protocol 1.0**
Corrected Spec Ver.	

Submission info

Name	Company	Date
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Description of the specification technical flaw (add space as needed)

The Byte Address specified in section 5.2 for a few of the Status and Control registers is incorrect. Specifically, the Byte Addresses are incorrect for registers 16-23. This erratum corrects these Byte Address ranges.

Description of the correction

Figure 34 in section 5.2 shall be updated as shown:

Register Index	Byte Address	Register Name	M/O	R/W	Description
0	80h	scrTempC	O	RO	Current temperature reading
1	84h	scrTempMaxP	O	RO	Peak maximum temperature reading
2	88h	scrTempMinP	O	RO	Peak minimum temperature reading
3	8Ch	scrStatus	O	RO	Status information for the device
4	90h	scrReallocsA	O	RO	Accumulated number of reallocated ATA sectors
5	94h	scrERetractsA	O	RO	Accumulated number of uncontrolled retracts
6	98h	scrCapabilities	M	RO	Capabilities and features of device
7-15	9Ch – BFh	Reserved	na	RO	Reserved for future definition
16	C0h ~~A0h~~	scrControl	M	RW	Control capabilities of device
17-23	C4h – DFh ~~A4h – DFh~~	Reserved	na	RW	Reserved for future definition
24-31	E0h – FFh	Vendor Specific	na	RW	Vendor specific registers

Key:
M/O = Mandatory/optional requirement.
M = Support of the register is mandatory.
O = Support of the register is optional.
R/W = Read/write support.
RO = The register is read-only.
RW = The register may be read or written.

Figure 34 Status and Control Register Map

Disposition log

04/11/2005	Erratum captured
07/11/2005	Erratum ratified